SRMS College of Engineering, Technology & Research, Bareilly

APRIL, 2017

CAMPUS-ANVESHAN

e- NEWSLETTER

EDITORIAL MEMBERS

CONTENTS

PRINCIPAL'S DESK

The Fourth Industrial Revolution

When we navigate through the various industrial revolutions the timelines appears as follow.

Revolution	Year	Information
1	1784	Steam, water, mechanical production equipment
2	1870	Division of labour, electricity, mass production
3	1969	Electronics, IT, automated production
4	?	Cyber-physical systems

The emergence of Fourth Industrial Revolution "cyber-physical systems" has already been perceived, It involves entirely new capabilities for people and machines powered by the capabilities of connectivity and internet with automation. While these capabilities are reliant on the technologies and infrastructure of the Third Industrial Revolution, the Fourth Industrial Revolution represents entirely new ways in which technology becomes embedded within societies and even our human bodies. Examples include genome editing, new forms of machine intelligence, breakthrough materials and approaches to governance that rely on cryptographic methods such as the blockchain.

The teaching learning systems of the institutions are expected to take active part in the upcoming industrial revolution

-Dr A K Srivastava

PUBLISHED BY

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EXPLORING THE SELF WITH DITATION: 13th April 2017

On 13th April, 2017 SRMSCET&R organized a stress reduction session on Topic "To reduce stress & increase efficiency with heart fullness meditations". The session was carried out by Dr. G.M. Bhatnagar and two of his colleagues from Shri Ramchandra mission. This session was mainly organized for the 1st year students to influence them to words meditation. Students learnt a lot of techniques for stress reduction. At last, Principal Sir addressed the gathering and a memento was presented to Dr. G.M. Bhatnagar.

SOFTWARE DEVELOPMNENT MARATHON:

22 April 2017

Believe that you will succeed and you will, with this moto SRMSCET&R has organized a Software Development Marathon dated on 22nd April, 2017 in which various students of Srmscet & r and Srmscet participated. The event started with the words of wisdom by Principal (Prof.) Dr. Anant Kumar Srivastava Sir. The event was about eradicating real life problems through innovative ideas of practical or theoretical model because the best way to predict the future is to create it. All the 60 participants presented their models and presentations very efficiently and gave assorted plan of their topic. Judges gave their decision on the basis of technology used effectively, modules, outcome, requirement gathering, future enhancement, user idea, flowchart, presentation skills and many more. The event was co-ordinate by the Verve (student activity welfare) Club.

The event ended with the distribution of certificates and prizes of Best Live Project and Best Idea and made the quote true that "Nothing will work unless you do."

FAREWELL 2017: 26 April 2017

SRMSCET&R organized farewell party *"Viva-La-Vida"* on April 26th, 2017 in the college auditorium where students of B.tech-3rd year bid farewell to the outgoing students of B.tech-4th year with great enthusiasm and off course nostalgia. The event started with the auspicious lamp lighting ceremony done by the Principal Prof. (Dr.)Anant Kumar Srivastava & all HOD's. Principal Sir wished good luck to the final year students for their future. He also expressed his hope that students will continue holding best positions in upcoming university exams.

Students of B.tech-3rd year presented very entertaining group dance and solo song performances. Special efforts were put into the presentations prepared by the students for the final year showing a glimpse of their Engineering life through photographs of college life and hostel. Some exciting games were also arranged for the students of final year like identify the person, silent disco etc. and were enjoyed by all. Token of love and appreciation was given to the students by their juniors along with beautiful Titles for them. The Trust Secretary, Aditya Murti Sir and Mrs. Richa Murti Ma'am too joined the event and graced it with their benign presence. Aditya Murti Sir highlighted few important points which a student can remember and recall after such ceremony.

He gave a little awakening to the students in terms of future endeavors and also was keen to help them in future interactions as alumni. Students performed duet dances which were especially dedicated to seniors. Students of final year participated in 'Fashion Parade' which was judged by Mrs. Richa Murti ma'am and other judges. Different tags were awarded to the students. Ms Priya Bhandari was crowned with the title of 'Ms Farewell' and Ms PrateekshaYadav was awarded the title of 'Ms Eveining' &Ms Simrat Kaur has been crowned as 'Ms. Popular'.In the end a heart touching drama showing different phases of "Engineering life @SRMS" was performed which took the seniors back to their college life and made the atmosphere emotionally surcharged.

HETEROGENEOUS – THE BENEFITS TO PERFORMANCE AND POWER CONSUMPTION

High-performance processors typically employ techniques such as deep, multi-issue pipelines, branch prediction and out-of-order processing to maximize performance, but these do come at a cost; specifically, they impact power efficiency. If some of these tasks can be parallelized, this impact could be mitigated by partitioning them across a number of efficient CPUs to deliver a high-performance, power-efficient solution. To accomplish this, CPU vendors have provided multi-core and multi-cluster solutions, and operating system and application developers have designed their software to exploit these capabilities.

Multi-threading

Even with out-of-order execution, with typical workloads, CPUs aren't fully utilized every CPU cycle; they spend the majority of their time waiting for access to the memory system. However, when one portion of the program (known as a thread) is blocked, the hardware resources could potentially be used for another thread of execution. This is why multi-threading can be so beneficial: the ability to switch to a second thread when the first thread is blocked leads to an increase in overall system throughput. Filling up all of the CPU cycles with useful work that otherwise would be un-used leads to a performance boost; depending on the application, the addition of a second thread to a CPU typically adds 40% to the overall performance, for an additional silicon area cost of around 10%. Hardware multi-threading is a feature that in CPU IP is bespoke to Imagination's MIPS CPUs.

(a) (b)

Fig: (a) Memory moves when transferring between clusters **(b)** Smaller, faster memory movement when transferring within a cluster

A common view

To move a task from one processor to another requires each processor to share the same instruction set and the same view of system memory. This is accomplished through shared virtual memory (SVM). Any pointer in the program must continue to point to the same code or data and any dirty cache line in the initial processor's cache must be visible to the subsequent processor.

Cache coherency

Cache coherency can be managed through software. This requires that the initial processor (CPU A) flush its cache to main memory before transferring to the subsequent processor (CPU B). CPU B then has to fetch the data and instructions back from main memory. This process can generate many memory accesses and is therefore time consuming and power hungry; this impact is magnified as the energy to access main memory is typically significantly higher than fetching from cache. To combat this, hardware cache coherency is vital, minimizing these power and performance costs. Hardware cache coherency tracks the location of these cache lines and ensures that the correct data is accessed by snooping the caches where necessary

Combining CPUs with dedicated accelerators

CPUs are general purpose machines. Their flexibility enables them to tackle almost any task but at the price of efficiency. Thanks to its optimizations, the PowerVR GPU is able to process larger, highly parallel computational tasks with very high performance and good power efficiency, in exchange for some reduction in flexibility compared to CPUs, and bolstered by a well-supported software development eco-system with APIs such as OpenCL or Open VX.Hardware acceleration can be coupled to the CPU by adding Single Instruction Multiple Data (SIMD) capabilities with floating point Arithmetic Logic Units (ALUs). However, while processing data through the SIMD unit, the CPU behaves as a Direct Memory Access (DMA) controller to move the data and CPUs make very inefficient DMA controllers.

Data transfer cost

To reduce time and energy costs, a Shared Virtual Memory with hardware cache coherency – as found in the I6500 CPU -- is ideal as it addresses much of the cost of transferring the task. This is because it eliminates the copying of data and the flushing of caches. There are other available techniques to achieve even greater reductions.

The benefits of heterogeneous

Multi-threaded, heterogeneous and coherent CPU clusters such as the MIPS I6500 have the ideal characteristics to sit at the heart of these systems. As such they are well placed to efficiently power the next generation of devices in many markets, such as ADAS and autonomous vehicles, networking, drones industrial automation, security, video analytics, machine learning and many others.

Source : www.computer.org

Compiled By:
Shikha Arya
Assistant professor (CS)

RIDDLE

1. A murderer is condemned to death. He has to choose between three rooms.

The first is full of raging fire

The second assassins with loaded guns

And the third, lions who have not eaten in years

Which room is the safest?

Ans. The third one is the safest, because the poor lions died of starvation.

2. This five letter word becomes shorter when you add two letters to it.

What is the word?

Ans. Short.

Shamama Kamal

CS 3rd year

Technology that can change the future

Wearable internet

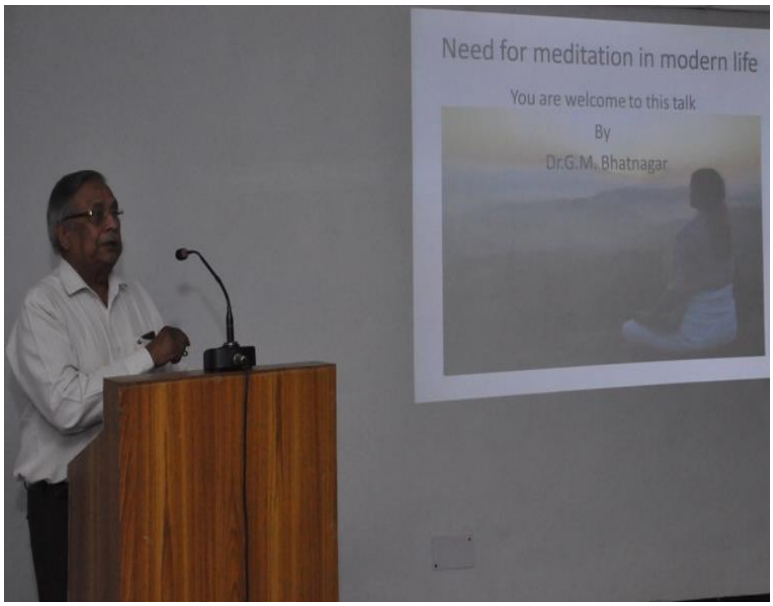
Technology is getting increasingly personal. Computers are moving from our desks, to our laps, to our pockets and soon they will be integrated into our clothing. By 2025, 10% of people are expected to be wearing clothes connected to the internet and the first implantable mobile phone is expected to be sold. Implantable and wearable devices such as sports shirts that provide real-time workout data by measuring sweat output, heart rate and breathing intensity are changing our understanding of what it means to be online and blurring the lines between the physical and digital worlds. The potential benefits are great, but so are the challenges. These devices can provide immediate information about our health and about what we see, or help locate missing children. Being able to control devices with our brains would enable disabled people to engage fully with the world. There would be exciting possibilities for learning and new experiences.

Source: World Economy Forum

NEWS IN PICTURE

SOME GLIMPSES

WORKSHOP ON EXPLORING THE SELF WITH MEDITATION



FAREWELL 2017